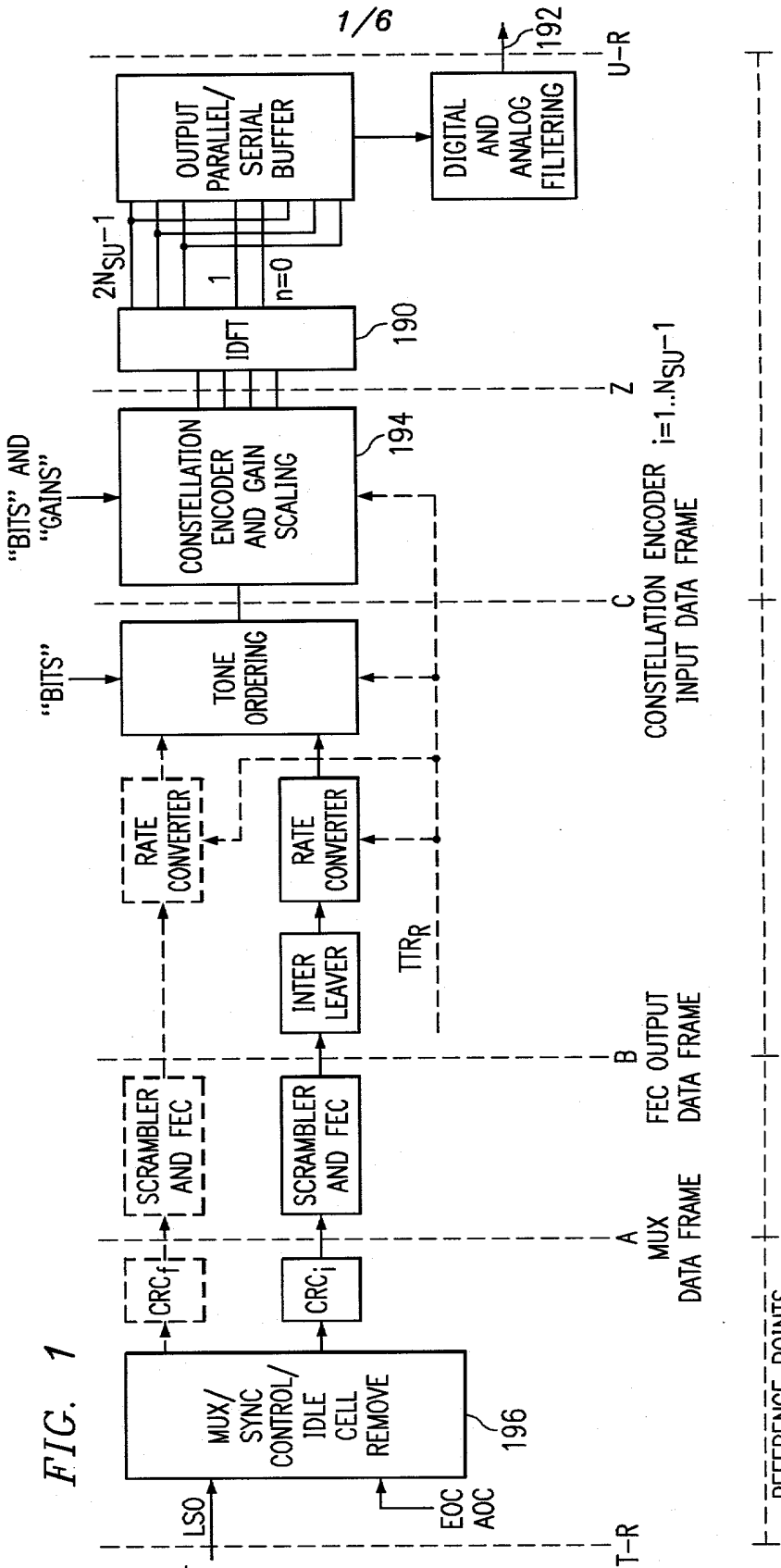

INPUT DATA
LSO
T-R
MUX/ SYNC CONTROL/ IDLE CELL REMOVE
196
EOC
AOC
CRC$_f$
CRC$_i$
SCRAMBLER AND FEC
SCRAMBLER AND FEC
A
MUX DATA FRAME
INTER LEAVER
RATE CONVERTER
RATE CONVERTER
TTR$_R$
B
FEC OUTPUT DATA FRAME
"BITS"
TONE ORDERING
"BITS" AND "GAINS"
CONSTELLATION ENCODER AND GAIN SCALING
194
C
CONSTELLATION ENCODER INPUT DATA FRAME
IDFT
190
Z
$2N_{SU}-1$
1
n=0
OUTPUT PARALLEL/ SERIAL BUFFER
DIGITAL AND ANALOG FILTERING
192
U-R
REFERENCE POINTS
i=1..$N_{SU}-1$

FIG. 1

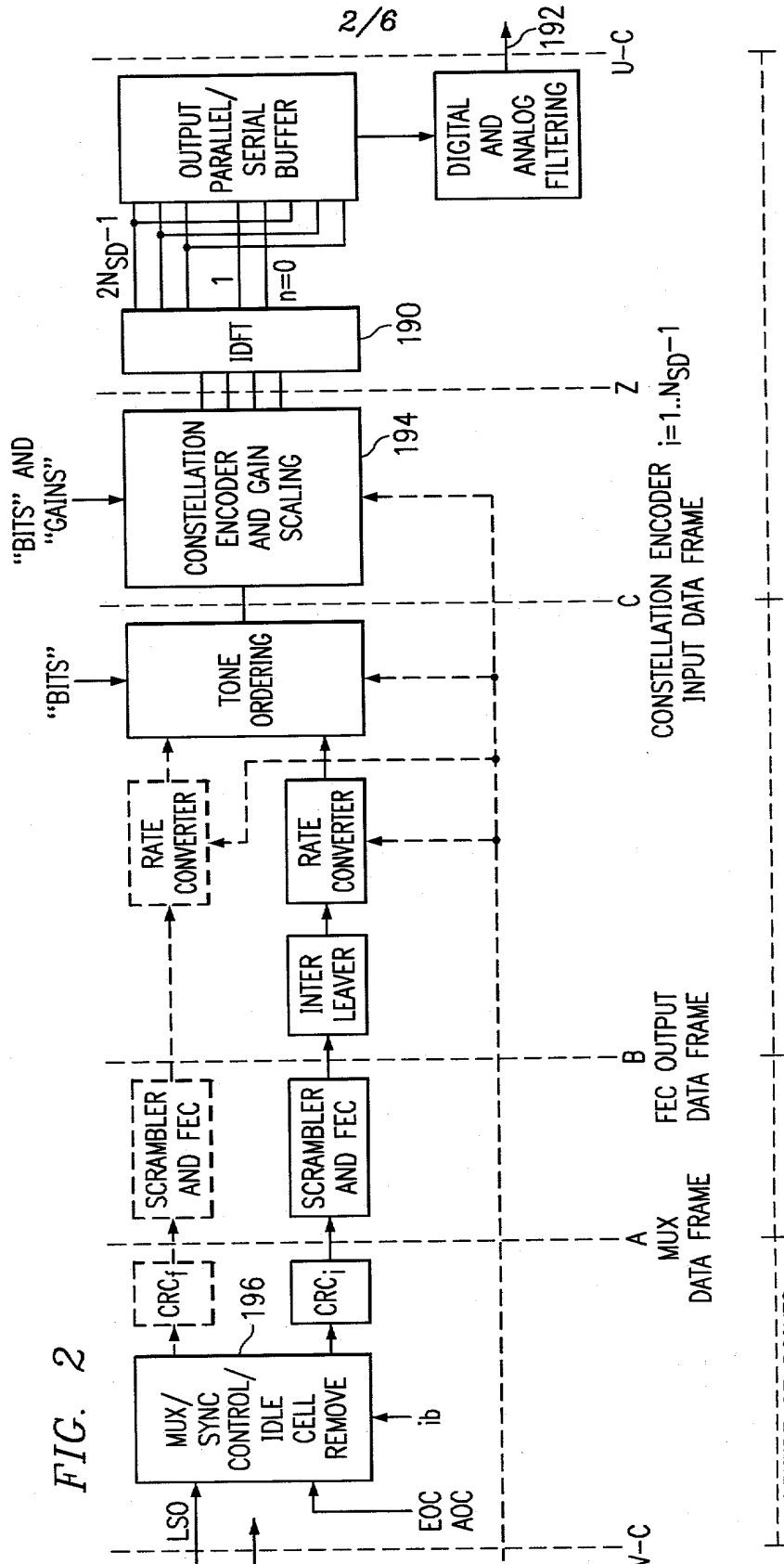

INPUT DATA
OAM
LSO
EOC
AOC
MUX/ SYNC CONTROL/ IDLE CELL REMOVE
ib
196
CRCf
CRCi
SCRAMBLER AND FEC
SCRAMBLER AND FEC
INTER LEAVER
RATE CONVERTER
RATE CONVERTER
"BITS"
"BITS" AND "GAINS"
TONE ORDERING
CONSTELLATION ENCODER AND GAIN SCALING
194
IDFT
190
2NSD-1
1
n=0
OUTPUT PARALLEL/ SERIAL BUFFER
DIGITAL AND ANALOG FILTERING
192
V-C
A
MUX DATA FRAME
B
FEC OUTPUT DATA FRAME
C
CONSTELLATION ENCODER INPUT DATA FRAME
Z
i=1..NSD-1
U-C
REFERENCE POINTS

FIG. 2

FIG. 3

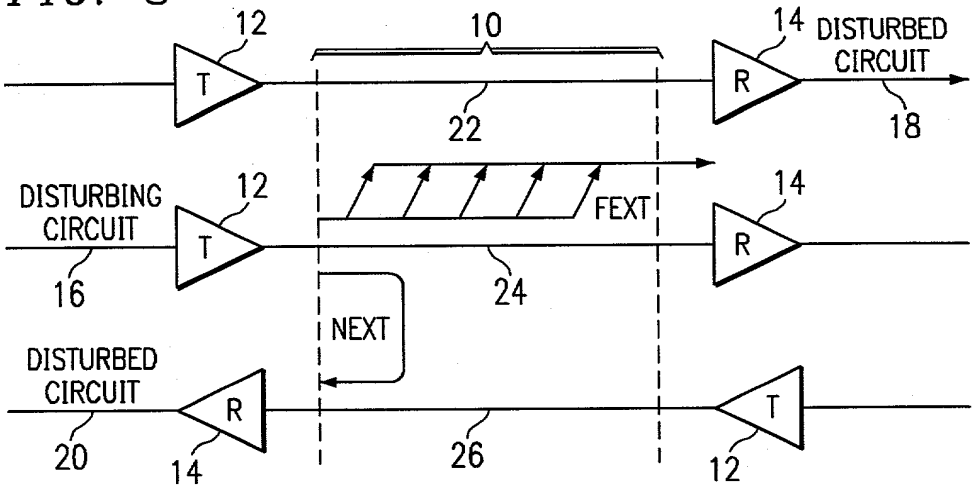


FIG. 5

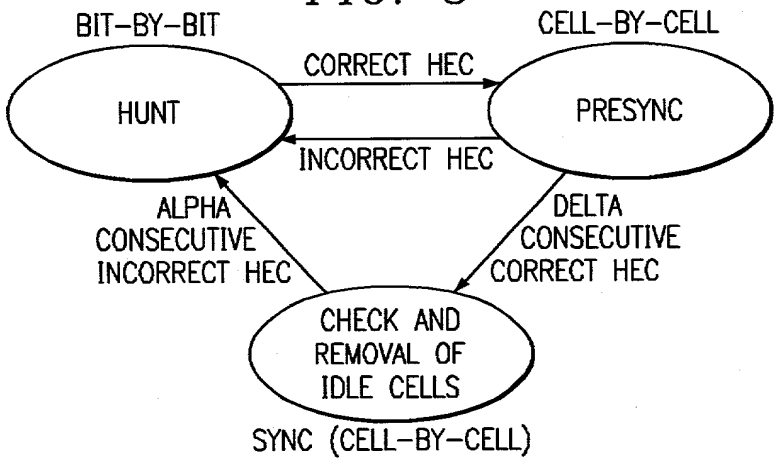


FIG. 4

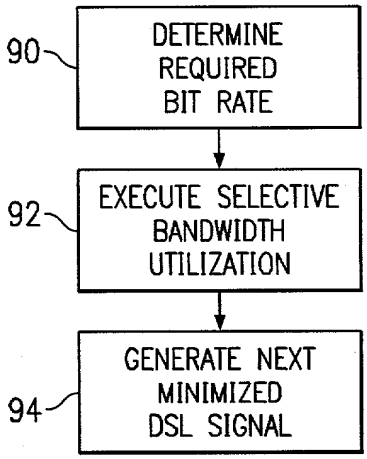


FIG. 10

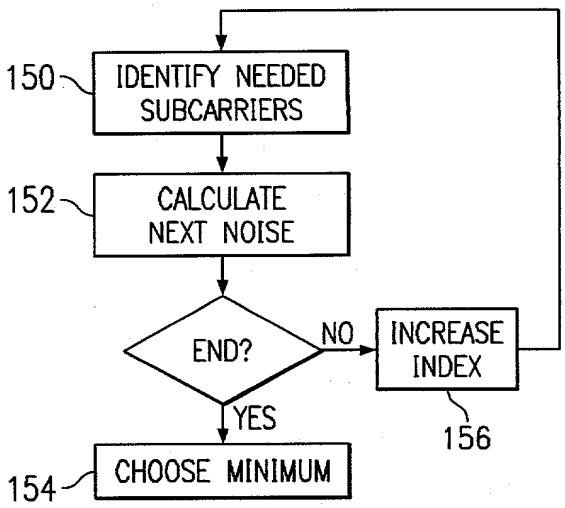


FIG. 6

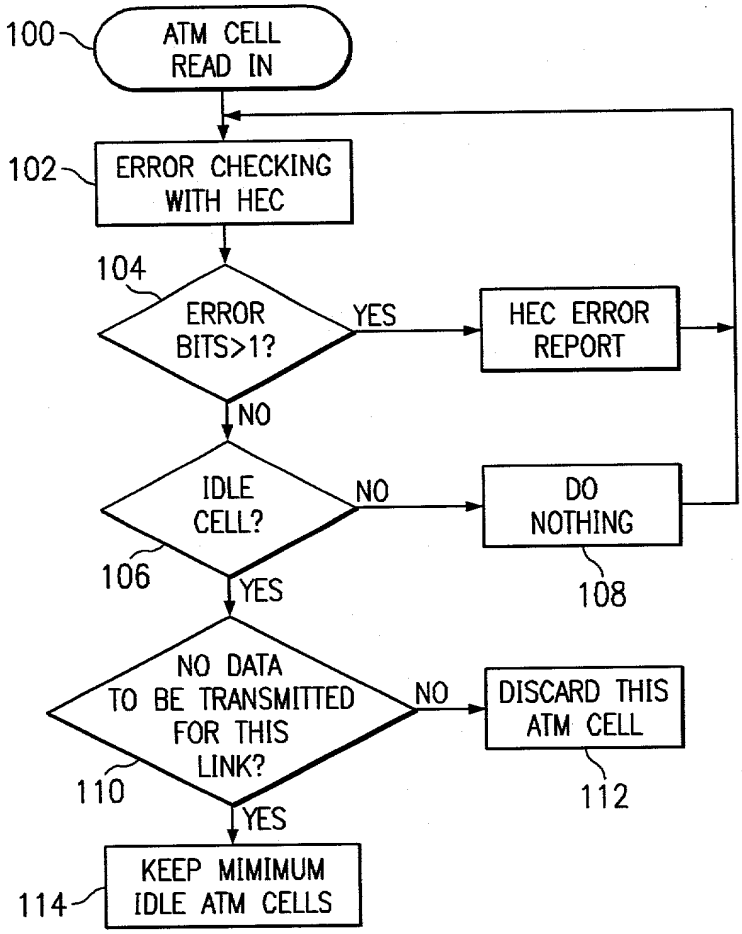

100
ATM CELL READ IN
102
ERROR CHECKING WITH HEC
104
ERROR BITS>1?
YES
HEC ERROR REPORT
NO
IDLE CELL?
NO
DO NOTHING
106
108
YES
NO DATA TO BE TRANSMITTED FOR THIS LINK?
NO
DISCARD THIS ATM CELL
110
112
YES
KEEP MIMIMUM IDLE ATM CELLS
114

FIG. 7

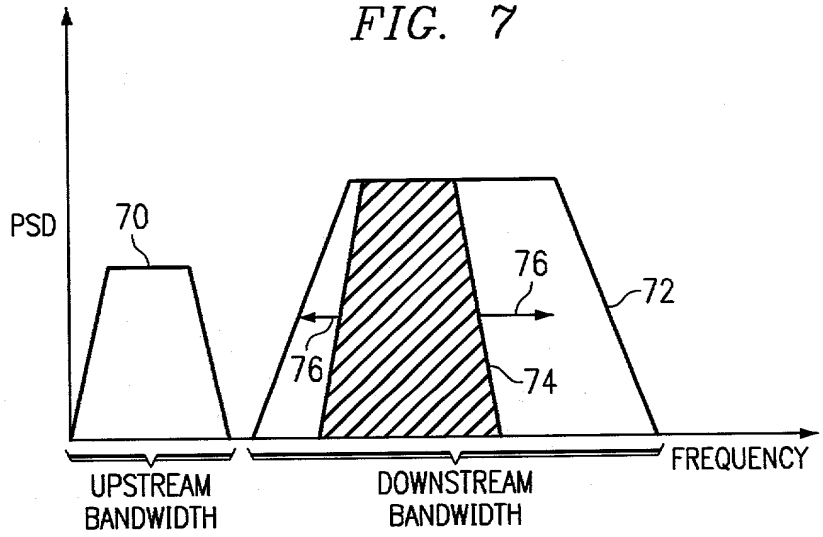

PSD
70
76
72
76
74
FREQUENCY
UPSTREAM BANDWIDTH
DOWNSTREAM BANDWIDTH

FIG. 8

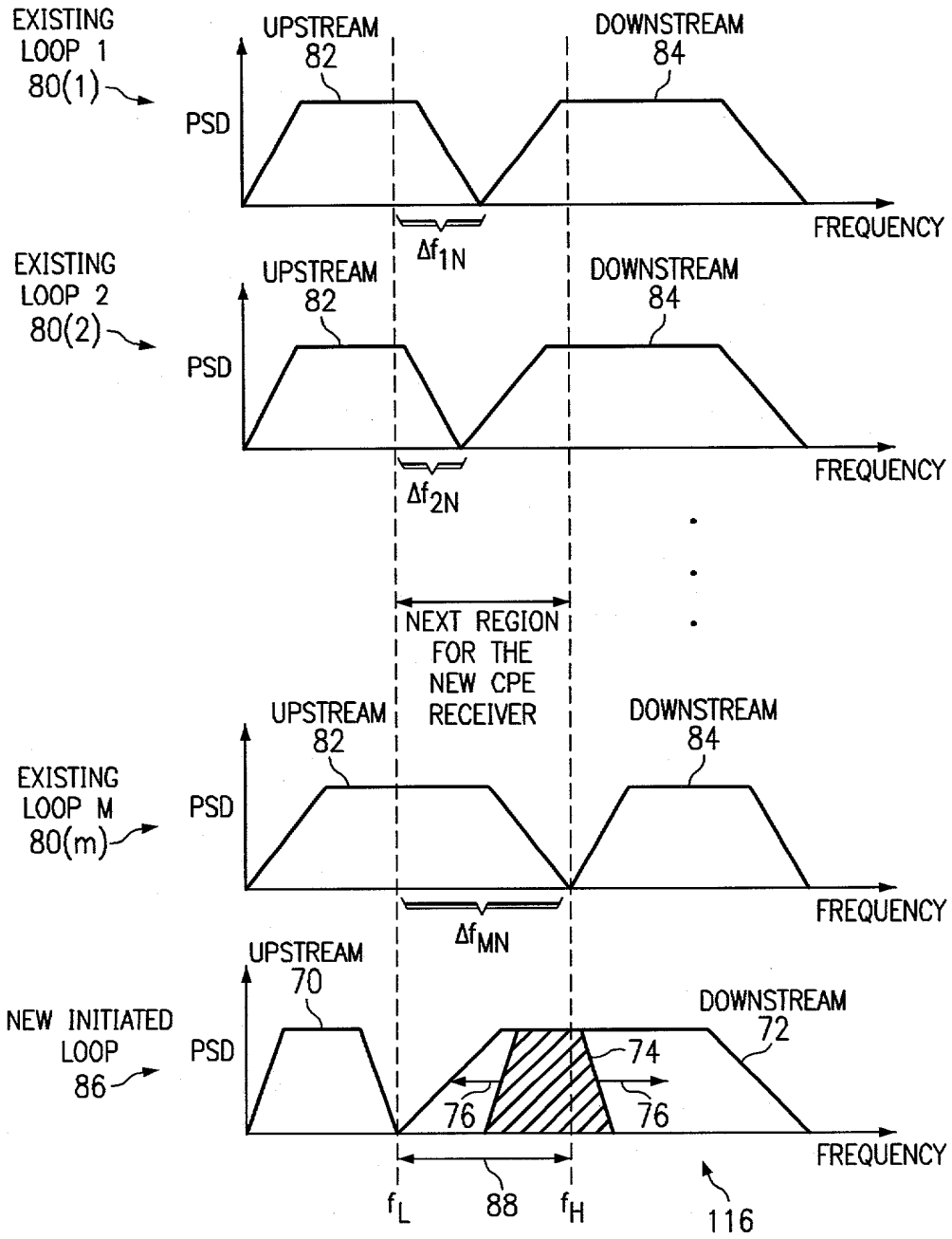
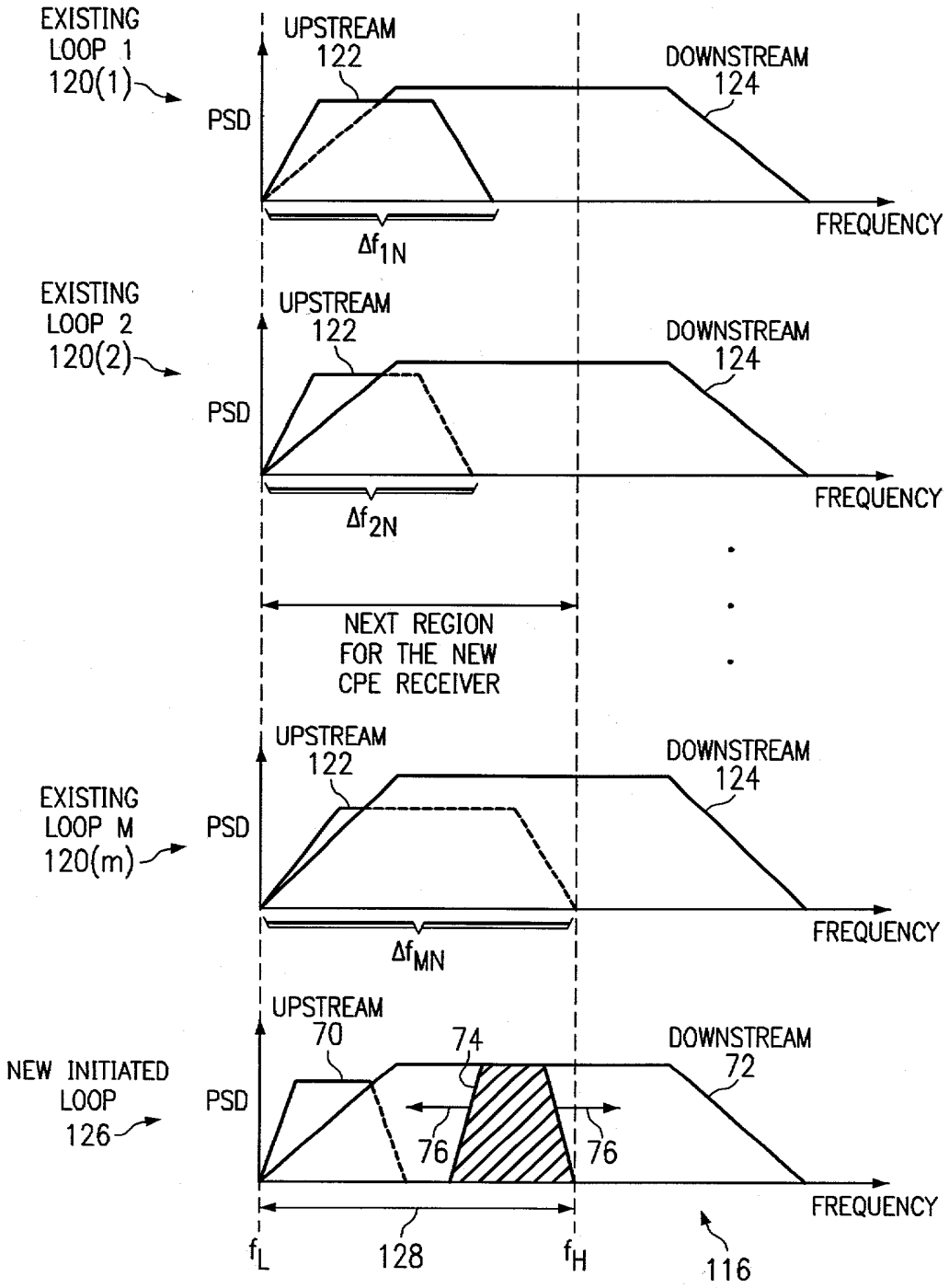

EXISTING LOOP 1 80(1)
UPSTREAM 82
DOWNSTREAM 84
PSD
FREQUENCY
Δf_{1N}
EXISTING LOOP 2 80(2)
UPSTREAM 82
DOWNSTREAM 84
PSD
FREQUENCY
Δf_{2N}
NEXT REGION FOR THE NEW CPE RECEIVER
EXISTING LOOP M 80(m)
UPSTREAM 82
DOWNSTREAM 84
PSD
FREQUENCY
Δf_{MN}
NEW INITIATED LOOP 86
UPSTREAM 70
DOWNSTREAM 72
PSD
74
76
76
FREQUENCY
f_L
88
f_H
116

FIG. 9


EXISTING LOOP 1 120(1)
UPSTREAM 122
DOWNSTREAM 124
PSD
FREQUENCY
Δf_{1N}
EXISTING LOOP 2 120(2)
UPSTREAM 122
DOWNSTREAM 124
PSD
FREQUENCY
Δf_{2N}
NEXT REGION FOR THE NEW CPE RECEIVER
EXISTING LOOP M 120(m)
UPSTREAM 122
DOWNSTREAM 124
PSD
FREQUENCY
Δf_{MN}
NEW INITIATED LOOP 126
UPSTREAM 70
74
DOWNSTREAM 72
PSD
76
76
FREQUENCY
f_L
128
f_H
116